The XDPP1100 FAQ

About this document

# Scope and purpose

This document lists the frequency asked questions and answers of the XDPP1100 digital controller.

# Intended audience

Infineon technical support center/ FAE/ sales

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# Hardware related questions

## What is the resolution of VOUT setpoint?

The LSB of Vout setpoint is determined by the larger value of the two:

1) LSB per VOUT\_MODE

2) 156.25 µV/VOUT\_SCALE\_LOOP

## How frequent the ADC updates? Does it require PWM trigger?

The AFE1 sample rate is 50 Msps. It is independent to the PWM edge or phase.

### How much voltage is allowed between VREF and GND?

+/- 300 mV.

## AFE2 9-bit ADC, why the input voltage range is less than 512\* 1.45mV?

Some ADC codes are used for offset trim thus the input voltage range is less than 512 \* 1.45 mV.

### Can I have common mode offset to the ISEN/IREF pin?

Yes, you can have common mode offset to ISEN/IREF.

### What is the maximum output current capability?

The XDPP1100 supports IOUT telemetry up to 128A. User could write FW patch to modify the resolution of output current and increase the range of maximum IOUT. FW patch example code is available.

## What is the current sharing algorithms?

By voltage droop or by active current sharing (IMON). See details in application note **Error! Reference source not found.**.

### What is bandwidth of active current sharing?

It is a slow loop. About 10% of voltage loop bandwidth.

### Does active current sharing modify the duty cycle or the reference?

Modify duty-cycle.

### Will peak current mode make current sharing simple?

The peak current mode is for loop control. It won’t affect secondary current sense and current sharing. So it has the same current sharing performance as voltage mode control.

## How many parallel loops can you implement?

A single IC (XDPP1100-Q040K64) supports up to two loops.

For multiple XDPP1100 in parallel, it supports up to 16 address offsets.

### Can dual-loop share current?

The dual-loop configuration has two independent loops and they don’t have internal current sharing.

## Does each AFE have comparator for fault protection?

Yes, details please see application note **Error! Reference source not found.**.

### Vout OVP fault delay time

The Vout fault comparator operates at 50 Mhz. Customer could configure the number of fault count. The fastest response could made within 50ns.

### How to prevent OVP when output resistor is open or short?

The XDPP1100 implements two types of open-sense protection. Please see application note **Error! Reference source not found.**.

## Input feed-forward mechanism

The XDPP1100 feed-forward is implemented by computing duty-cycle based on Vin and Vout voltage. The feed-forward is implemented by hardware.

### How fast is the feed-forward response?

By default the feed-forward is updated every switching cycle. User could also configure the high speed feed-forward by enabling the same cycle mode (vrs\_same\_cycle\_en) for 20ns response. Details see application note **Error! Reference source not found.**.

### Can I use VRSEN to sense DC input voltage?

Yes. The VRSEN can be configured to DC mode. Set vsp1\_vrs\_sel = 0 to configure VRSEN ADC to be the general ADC mode (DC mode).

## Is flux balancing implemented in hardware?

Yes.

## Is PID compensation implemented in hardware?

PID is implemented in hardware.

### What types of PID compensation?

One pole, two zeros, with two additional poles by pre and post filter.

### How fast does IC calculate PID?

The PID is calculated at 50 Mhz clock.

### Does IC adjust duty cycle every a switching period or every half switching period?

For bridge topologies, the duty cycle is adjusted every half switching period. But if the rampX\_dutyc\_lock register is set to 1, the even cycle will have the same duty as the odd cycle.

## Can I use VD12 as voltage reference?

No. The 1.2V is the power supply for internal digital circuit. It is not intend to be used as a voltage reference.

## What is the frequency setpoint accuracy?

Tsw resolution is 20ns. It is recommended to set the switching frequency to make Tsw = integer x 20ns. For example, if the user want to set switching frequency around 300khz. Set it to 301khz will result higher set point accuracy rather than set it to 300khz.

The frequency variation over temperature -40 °C to 125 °C is +/-5%.

## Can it accept an analog voltage as a reference for Vo?

With FW patch user could apply a voltage on General ADC pin (i.e. PRISEN), digitize it with the TS ADC and use this to drive the target output voltage instead of the PMBus VOUT\_COMMAND.

## Can the GPIO pins support a 15MHz clock/data rate?

Yes, but firmware would be rather limited in BW at that speed if bit banging all of the time.  If we are talking about short bursts at 15 Mhz it would be fine.

## Can I use the XADDR1 pin as a general ADC input?

Yes. The current source of the XADDR1 is only enabled during the initialization when IC obtains the address offset. The current source would be disabled by FW after the address decoding. Please note when using the XADDR1 as ADC input, the input voltage range should be 0V ~ 1.2V.

## What is the satus of PWM during power up and FW reset?

The PWM is in Hi-Z (high impedance) mode during initial boot and during FW reset. After initialization, register configuration would be downloaded from OTP to RAM and the status of PWM would change depend on configuration (open-Drain or push-pull). Default config has all the PWM pins configured as PWM output with push-pull (CMOS) output.

# Firmware related questions

## FW develop environment

XDPP1100 Integrated Development Environment (IDE) is equipped with both GCC compiler and ARM-CC compiler. However, GCC is set to be the default compiler.

### Is ARM compiler license included with the device?

No. Customers need to buy their licenses for code development.

## Is there Flash available in this device?

No. The XDPP1100 offers OTP for user data and firmware patch storage.

## How many times can OTP be programmed?

OTP is One Time Programming memory. The XDPP1100 has 64kB OTP for user to store configuration and FW patch. User could change the OTP partition for data config and FW patch code.

The data partition can be set up to 31kB. If the configuration doesn’t have extra user defined MFR PMbus commands, the size is about 2kB for 2-loops. The 31kB OTP could be programmed up to 15 times.

If there is FW patch to be stored into OTP, the number of re-write depends on the size of the patch code. The old patch must be invalidate before storing new patch to the same partition.

During debugging, user should use RAM to verify the FW patch code and configuration. Customer can change the configuration as many times as needed. However, the configuration will be lost after power down 3.3V. Please save the configuration to a design file before power cycle the 3.3V VDD.

Once the configuration is finalized, user could store the config to OTP for production.

## Can I test my FW patch in RAM?

Sure you can.

## What RAM size is available for customer to use?

The XDPP1100 has 32 kB RAM. 22 kB is used for ROM code running. User can use 10 kB for customized FW patch and patch data. By default, the RAM is configured 8 kB for patch code and 2 kB for patch data.

## What if my patch size is larger than 8kB, can I still test it in RAM?

If you have larger patch code, you can modify RAM configuration for 9kB patch code and 1kB patch data. The RAM address starts at 0x20061800, ends at 0x20063FFF. The patch data is reserved in the last 2kB. Modify partial\_patch.cfg file to change the patch data start\_address from 0x20063800 to 0x20063C00. It will allow 9kB patch.

Since it requires minimum 1kB for patch data, a patch larger than 9kB will not work in RAM. You have to choose “store to OTP” if the patch size is larger than 9kB.

By default, the OTP Section 1 Size has been configured as 0xC000 (48 KB) in the XDPP1100 GUI. To store OTP effectively, users are encouraged to modify the OTP Section Size according to the Firmware Patch Size.

## Can I store more than one FW patch into OTP?

XDPP1100 allows storing multiple FW patches at different partition in the OTP. This is done by selecting the Partition Number in the XDPP1100 GUI. However, there can only be one active patch running in the OTP and this is the partition with the lowest number.

## Are the Boot and FW code programmed in ROM in factory?

Yes.

## Can I2C recover from lockup

Yes. The XDPP1100 has timeout mechanism implemented. 30ms bus timeout and 5us clock stretch timeout.

I2C lockup, means if there are slave devices connected to the I2C bus (EEPROM for example), and the Slave does not have reset function. In an abnormal condition, the SDA could be stuck low. Both Master and Slave will wait for each other forever. The master device (XDPP1100) should have auto-recovery function which monitors SDA, and initiate SCL clock if the SDA stuck low after reset.

## Can Infineon open source code?

All the firmware APIs from Hardware-Abstraction-Layer to the Application-Layer are available as header files and come with documentation. Firmware patch development workflow make use of these APIs and documentation. The source codes implemented in the APIs are kept as close-source due to proprietary IPs.

## Can I update FW while the loop is in regulation?

It depends on what the firmware update is.  If it is unrelated to the regulation then it is possible but definitely not recommended.

## Failed to generate MFR PMBus command using Shasta\_pmbus.xlsx

Please check that the Python path is set correctly in the PMBus Makefile: {Project}/common/MakefilePmbus.mk. Another root cause is due to the EXCEL default language. Please change it to English.

## What is the meaning of UX.Y data format?

In the unsigned UX.Y format, X defines to position and weight of the most significant bit (MSB) and Y defines the position and weight of the least significant bit (LSB).

X defines weight of the MSB as 2^(X-1).  It can also be thought of as the binary point position in terms of bits to the right of the MSB.  When X and Y are both >= 0, it also corresponds to the number of bits to the left of the binary point (i.e., number of integer bits).

Y defines the weight of the LSB as 2^(-Y).  It can also be thought of as the binary point position in terms of bits to the left of the LSB.  When X and Y are both >= 0, it also corresponds to the number of bits to the right of the binary point (i.e., number of fractional bits).

With this definition it falls out that X + Y = total # bits.

Some examples:

U8.6 :

MSB weight = 2^(8-1) = 2^7, LSB weight = 2^-6, # bits = 8 + 6 = 14.

Binary point position = xxxxxxxx.yyyyyy, bp is 8 bits to right of MSB and 6 bits to left of LSB.

U8.0 :

MSB weight = 2^(8-7) = 2^7, LSB weight = 2^-0 = 2^0, # bits = 8 + 0 = 8.

Binary point position = xxxxxxxx.0, bp is 8 bits to right of MSB and 0 bits to left of LSB

U8.-2 :

MSB weight = 2^(8-1) = 2^7, LSB weight = 2^2, # bits = 8 + -2 = 6.

Binary point position = xxxxxx00.0, bp is 8 bits to right of MSB and -2 bits to left of LSB

U0.6 :

MSB weight = 2^(0-1) = 2^-1, LSB weight = 2^-6, # bits = 0 + 6 = 6.

Binary point position = 0.yyyyyy, bp is 0 bits to right of MSB and 6 bits to left of LSB

U-2.6 :

MSB weight = 2^(-2-1) = 2^-3, LSB weight = 2^-6, # bits = -2 + 6 = 4.

Binary point position = 0.00yyyy, bp is -2 bits to right of MSB and 6 bits to left of LSB

## What is the meaning of SX.Y data format?

The twos compliment signed SX.Y format essentially follows the same definition as UX.Y.  The “sign” bit is included in “X” and the weights and binary point positions are the same as for UX.Y.  The number of bits is still equal to X + Y.

## What is the meaning of 3E2M data format?

It means a 5-bit number with 3 bits Exponent and 2 bits Mantissa. The register map document description gives the real value equation whenever this notation is used.

## Which Python should I install?

Python 2.7.10.

## How do I start XDPP1100 IDE?

Go to installation folder (default is C:\XDPP1100), go to C:\XDPP1100\XDPP1100\_fw\ folder and click on “start\_eclipse.bat”.

## Which folder should I import into Eclipse workspace?

Assume the installation folder is C:\XDPP1100, import the contents from C:\XDPP1100\XDPP1100\_fw\projects\ into Eclipse workspace.

## Which project should I use as the base project for my patch development?

Use patch\_user\_app project as the base of your firmware development.

1. Open your project folder in file explorer (Assume default installation folder, the project folder is C:\XDPP1100\XDPP1100\_fw\projects\ )
2. Copy patch\_user\_app project folder and give a name to your project, e.g. “patch\_hello\_world”
3. Go in to your project folder and find .project file.
4. Replace the third line (you should see “patch\_user\_app”) and replace it with your project name “patch\_hello\_world”
5. Go back to Eclipse and then import the “patch\_hello\_world”

## Which file to be downloaded into OTP after compilation?

The compilation will produce .elf, .bin, .hex files. Download .bin file into the OTP.

# Peripheral

## Can I use PTC or BJT to sense temperature?

Yes, the XDPP1100 supports user defined temperature lookup table. It can be implemented in FW patch.

# GUI related questions

## Where can I download GUI?

myICP or Infineon toolbox.

## How to scan the I2C or PMBus address?

By default the I2c address and PMBus address is mapped to 0x10 and 0x40 (7 bit addresses and for 8 bit address = 0x20 and 0x80). Read from the register locations 0x70080044 and 0x70080048 to know about the i2c and PMBus address.

Since, you do not know the i2c address at this point, you scan from 0x08 to 0x7F and when you see ack on this one, then you can look further to find out the i2c and PMBus address like below.

    ack = i2cread4Bytesaddress2Bytesdata(address,0x44,0x00,0x08,0x70,4,&icversionID1[0]);

      if (ack == 0)

      {

            \*i2caddress = (((icversionID1[1] \* 64 )+ icversionID1[0]/4) & 0x7F);

            \*i2caddressfound = 1;

            ack = i2cread4Bytesaddress2Bytesdata(address,0x48,0x00,0x08,0x70,4,&icversionID1[0]);

            if (ack == 0)

            {

                  \*Pmbaddress = (((icversionID1[1] \* 64 )+ icversionID1[0]/4) & 0x7F);

                  \*Pmbusaddress = 1;

            }

            else

            {

                  \*Pmbusaddress = 0;

            }

            if (\*i2caddress == 0)

                  \*i2caddress = 0x10;

            if (\*Pmbaddress == 0)

                  \*Pmbaddress = 0x40;

      }

      else

      {

            \*Pmbusaddress = 0;

            \*i2caddressfound = 0;

      }

## What addresses need to be skipped when scanning addresses?

We scan between addresses 0x08 to 0x78 and skip the address (0x00 to 0x07, 0x0C, and 0x78 to 0x7F), using the skip radio button provided in the GUI.

# Nomenclature

1. Definitions of acronyms, symbols, and terms

| Symbol, Acronym, or Term | Definition |
| --- | --- |
| ACF | Active Clamp Forward |
| CRC | Cyclical Redundancy Checking |
| FBFB | Full-Bridge topology with full-bridge rectifier |
| FW | Firmware |
| GUI | Graphical User Interface |
| HBCT | Half-Bridge Center-Tap topology |
| HW | Hardware |
| LPF | Low Pass Filter |
| LSB | The Least Significant Bit |
| NTC | Negative Temperature Coefficient |
| OCP | Over current protection |
| OSP | Open Sense Protection |
| OTP | Over temperature protection |
| OTP | One Time Programmable memory |
| OVP | Over voltage protection |
| PCL | Peak Current Limit |
| PID | Proportional Integral Derivative |
| PTC | Positive Temperature Coefficient |
| PWM | Pulse width modulation |
| SCP | Short Circuit Protection |
| UCP | Under current protection |
| UTP | Under temperature protection |
| UVP | Under voltage protection |
| Vin | Input voltage |
| Vout | Output voltage |
| Vrect | Transformer secondary rectified voltage |

# List of application note

1. [XDPP1100 datasheet](https://www.infineon.com/dgdl/Infineon-XDPP1100-Q040-DataSheet-v02_00-EN.pdf?fileId=5546d462700c0ae6017084a8c9070d2a)
2. XDPP1100 GUI installation and user guide

1. [XDPP1100 application note](https://www.infineon.com/dgdl/Infineon-Application_guide_digital_power_controler_XDPP1100-ApplicationNotes-v02_00-EN.pdf?fileId=5546d46272e49d2a01730aa45d53481b)
2. XDPP1100 technical reference manual

Revision history

| Document version | Date of release | Description of changes |
| --- | --- | --- |
| Rev 1.0 | 2019-11-19 | Original document |
| Rev 1.1 | 2019-12-12 | Updated FW Q&A based on Halim’s input |
| Rev 1.2 | 2020-01-06 | Added GUI questions based on emails from Venu (Delta support)  Added FW questions of data format |
| Rev 1.3 | 2020-12-07 | Added Q2.16 to Q2.20 |
| Rev 1.4 | 2020-12-08  2020-12-11 | Updated chapter 6, the list of AppNote, added hyperlink to DS and AN.  Small update to Q2.3 |
|  | 2021-01-27 | Updated Q1.11, add frequency temperature variation spec  Added Q1.15, PWM status during initial boot and FW reset |